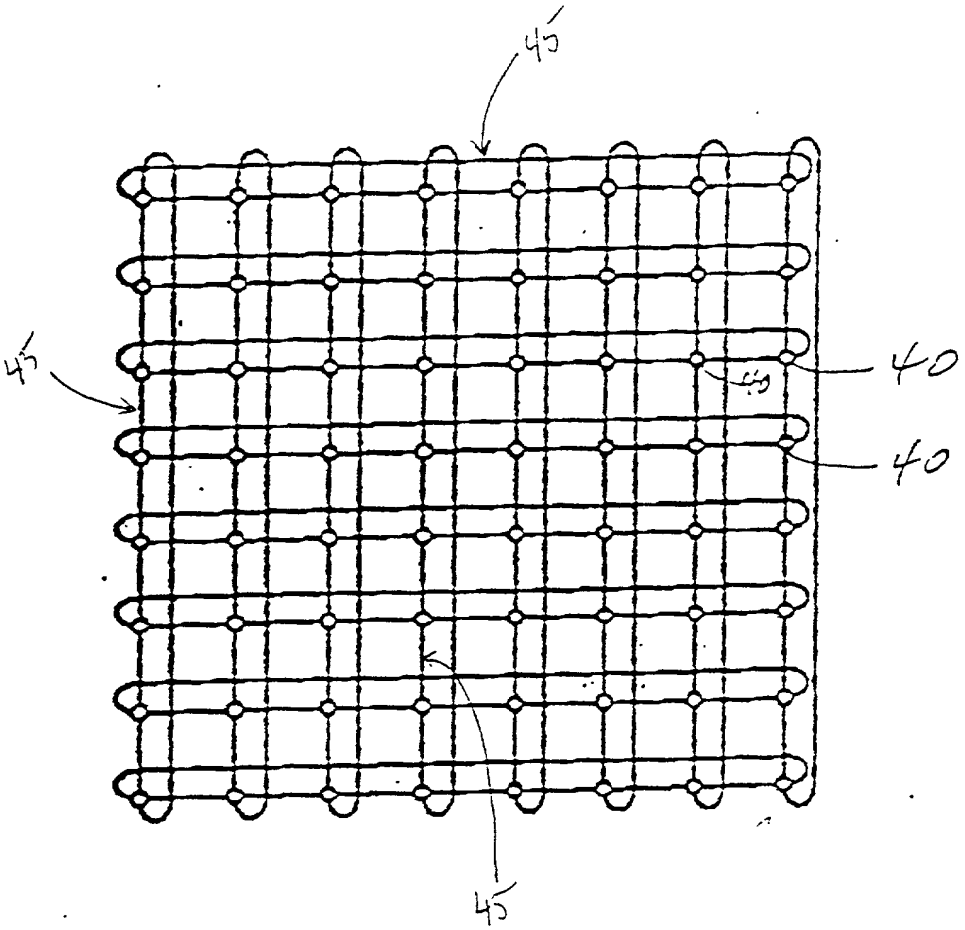


FIG. 1

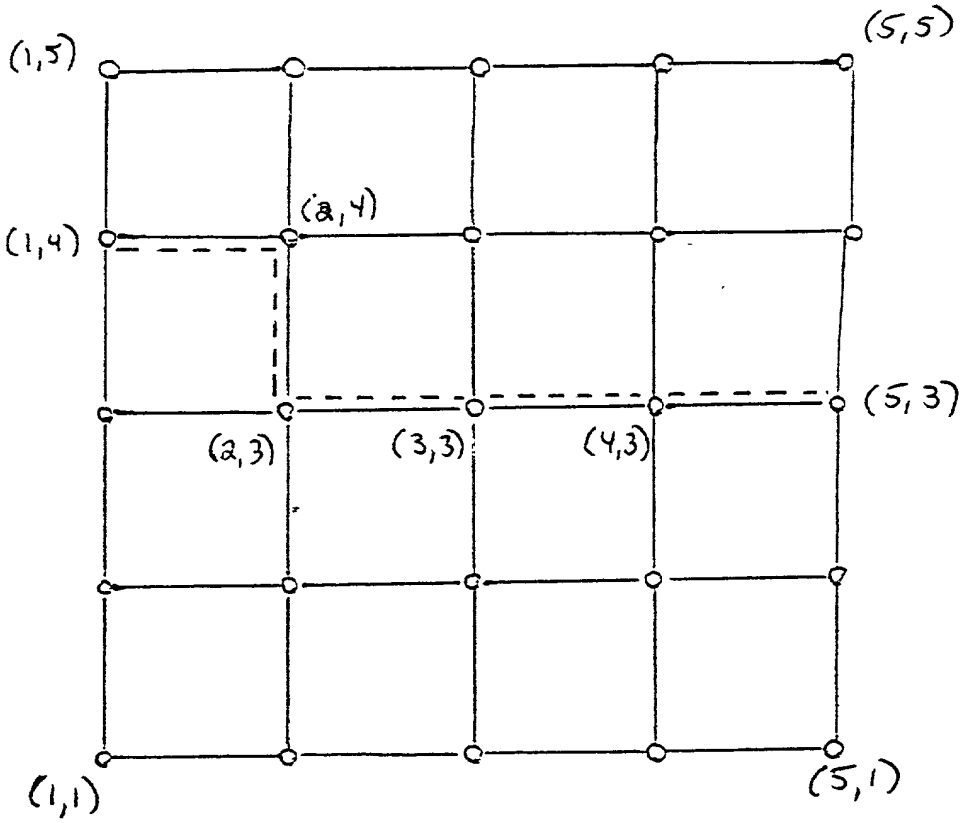


FIG. 2

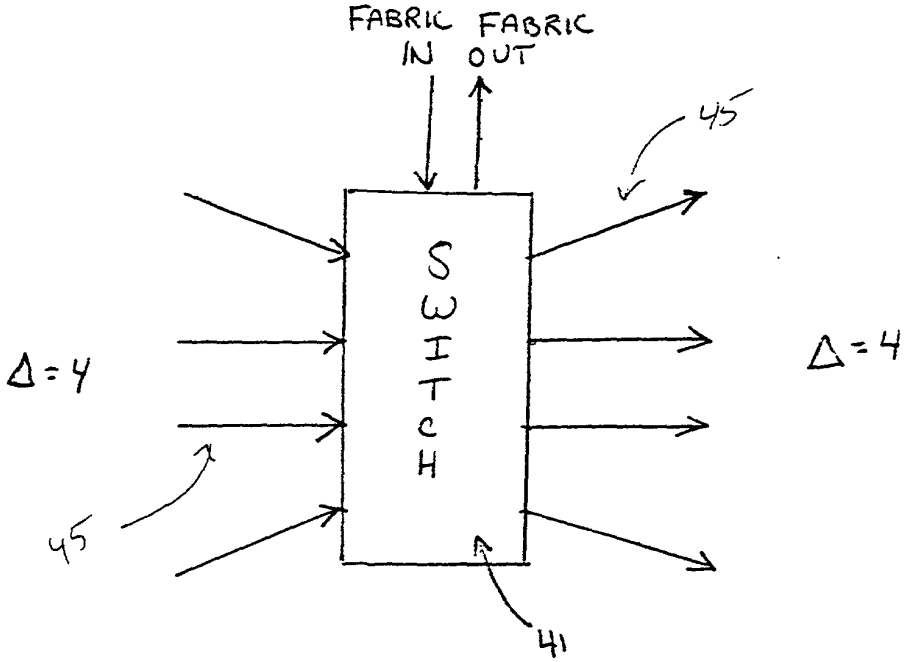


FIG. 3

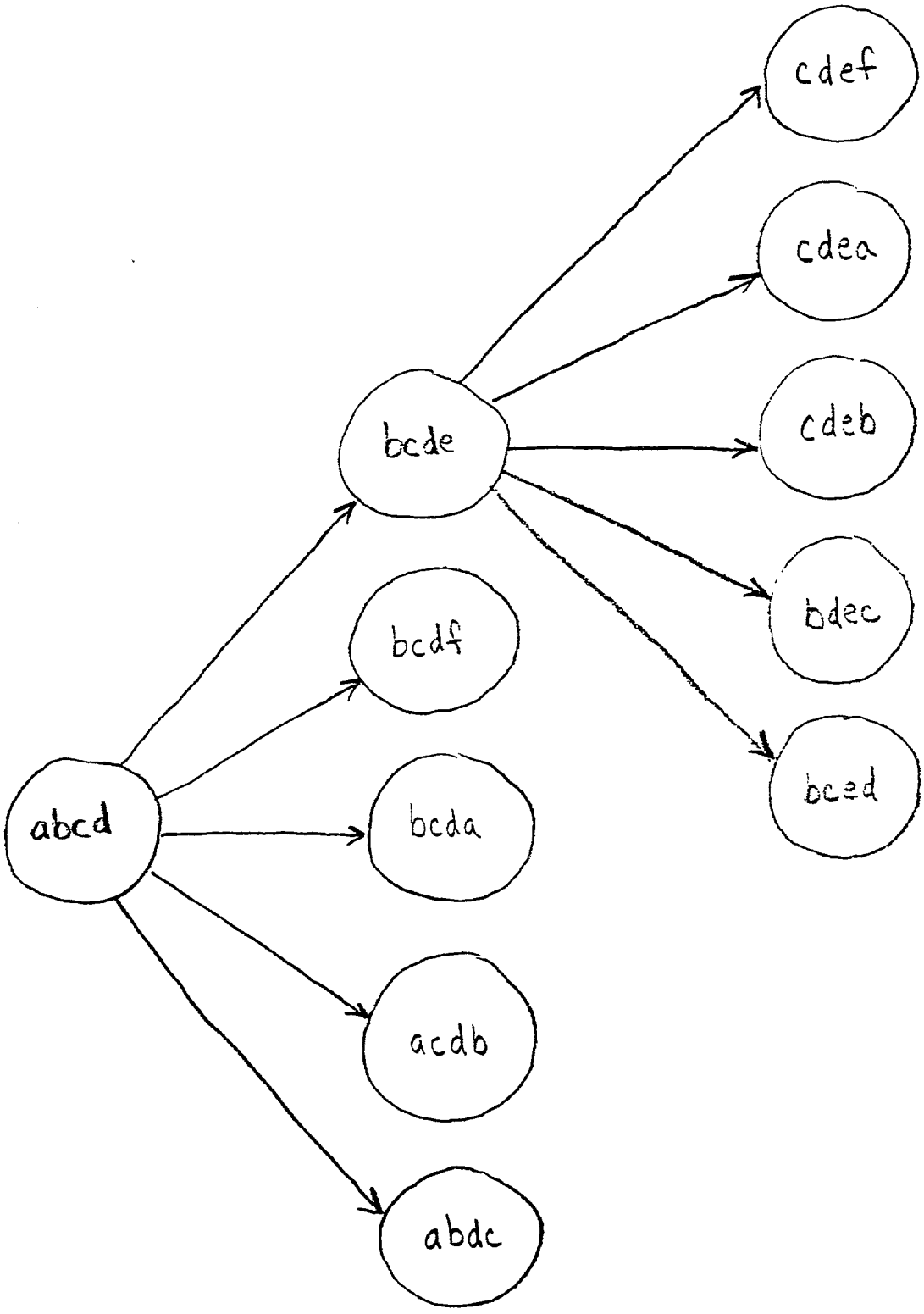


FIG. 4A

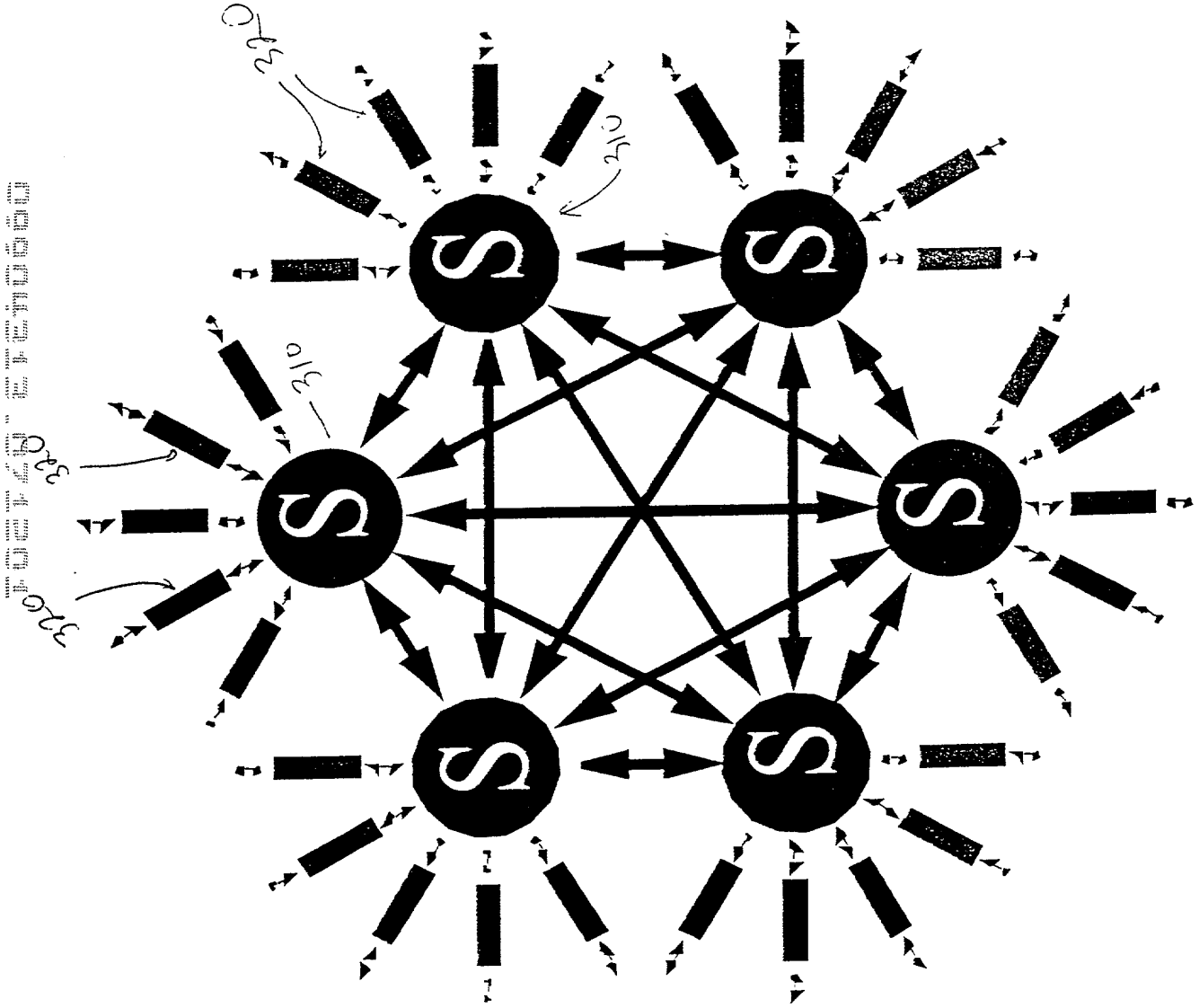
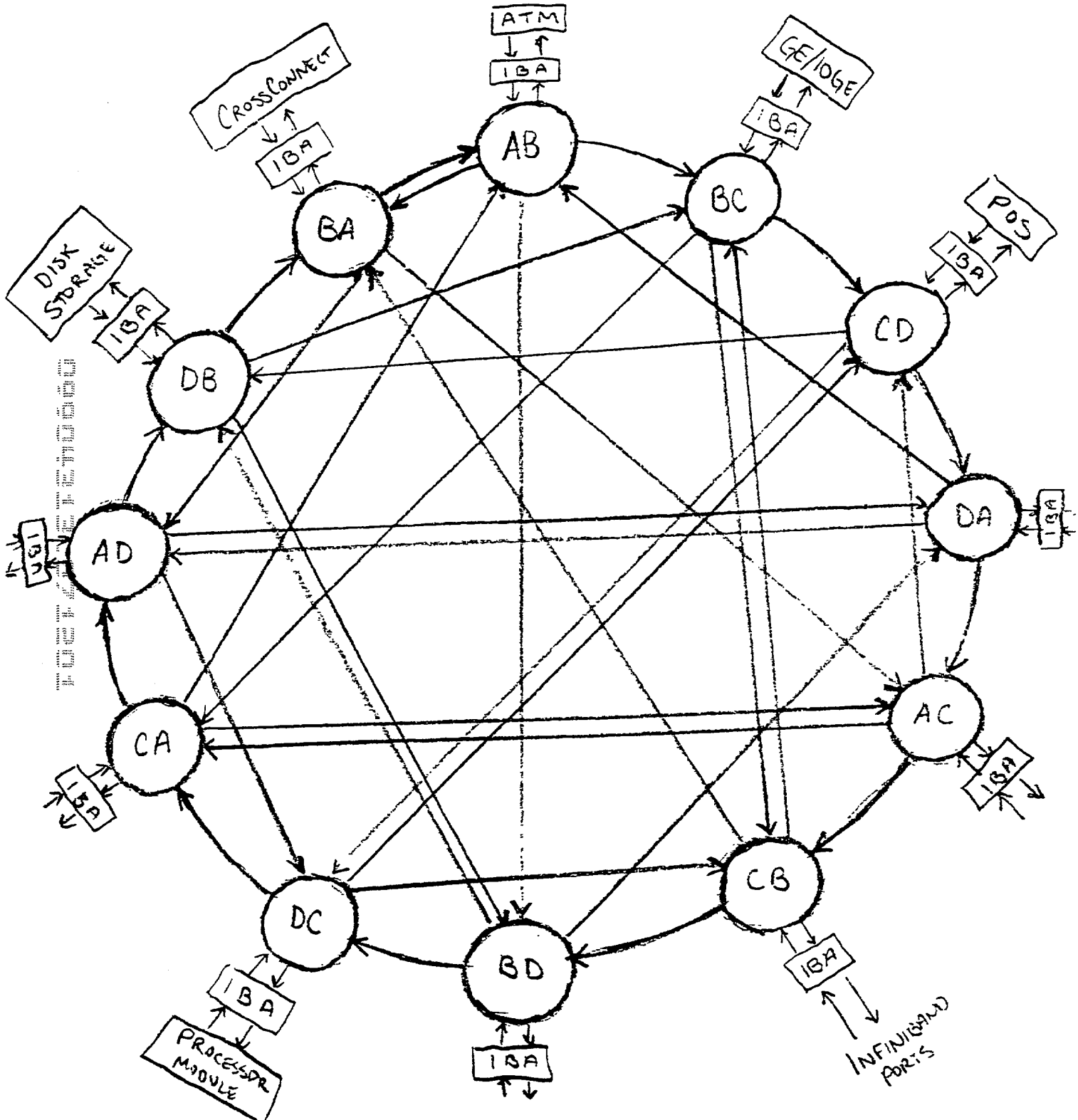


Fig. 4B



$\Delta = 3$
$D = 2$

FIG. 5A

ADJACENCY TABLES FOR NODES IN FIG. 5A

AB	**AC**	**AD**
AB → BC	AC → CB	AD → DB
AB → BD	AC → CD	AD → DC
AB → BA	AC → CA	AD → DA
BA	**BC**	**BD**
BA → AC	BC → CD	BD → DA
BA → AD	BC → CA	BD → DC
BA → AB	BC → CB	BD → DB
CA	**CB**	**CD**
CA → AB	CB → BD	CD → DA
CA → AD	CB → BA	CD → DB
CA → AC	CB → BC	CD → DC
DA	**DB**	**DC**
DA →AB	DB → BA	DC → CA
DA →AC	DB → BC	DC → CB
DA →AD	DB → BD	DC → CD

FIG. 5B

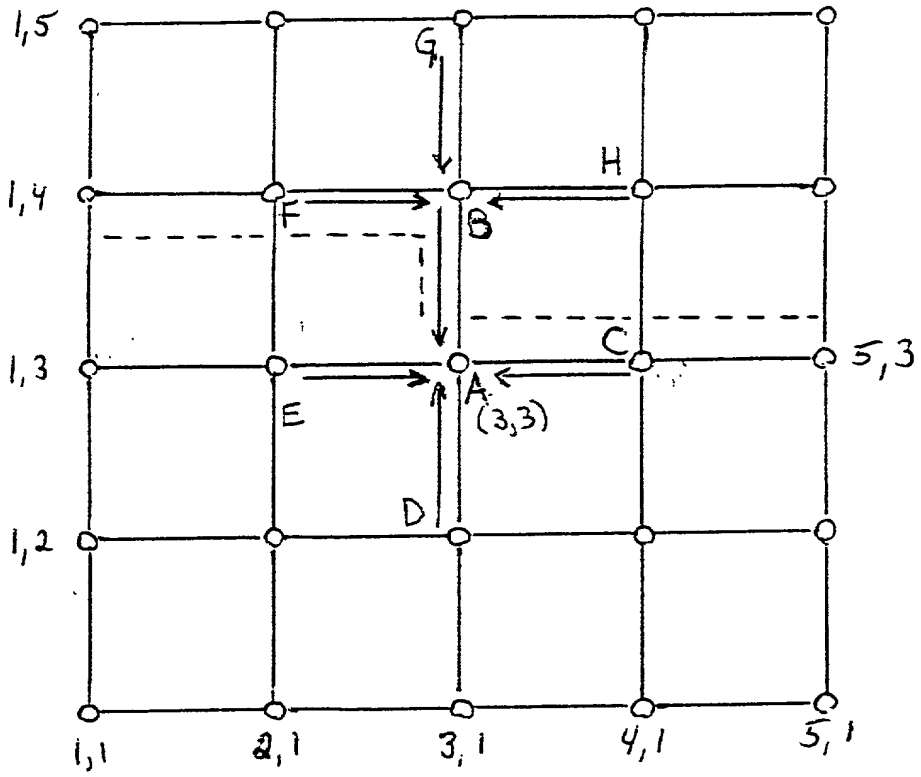
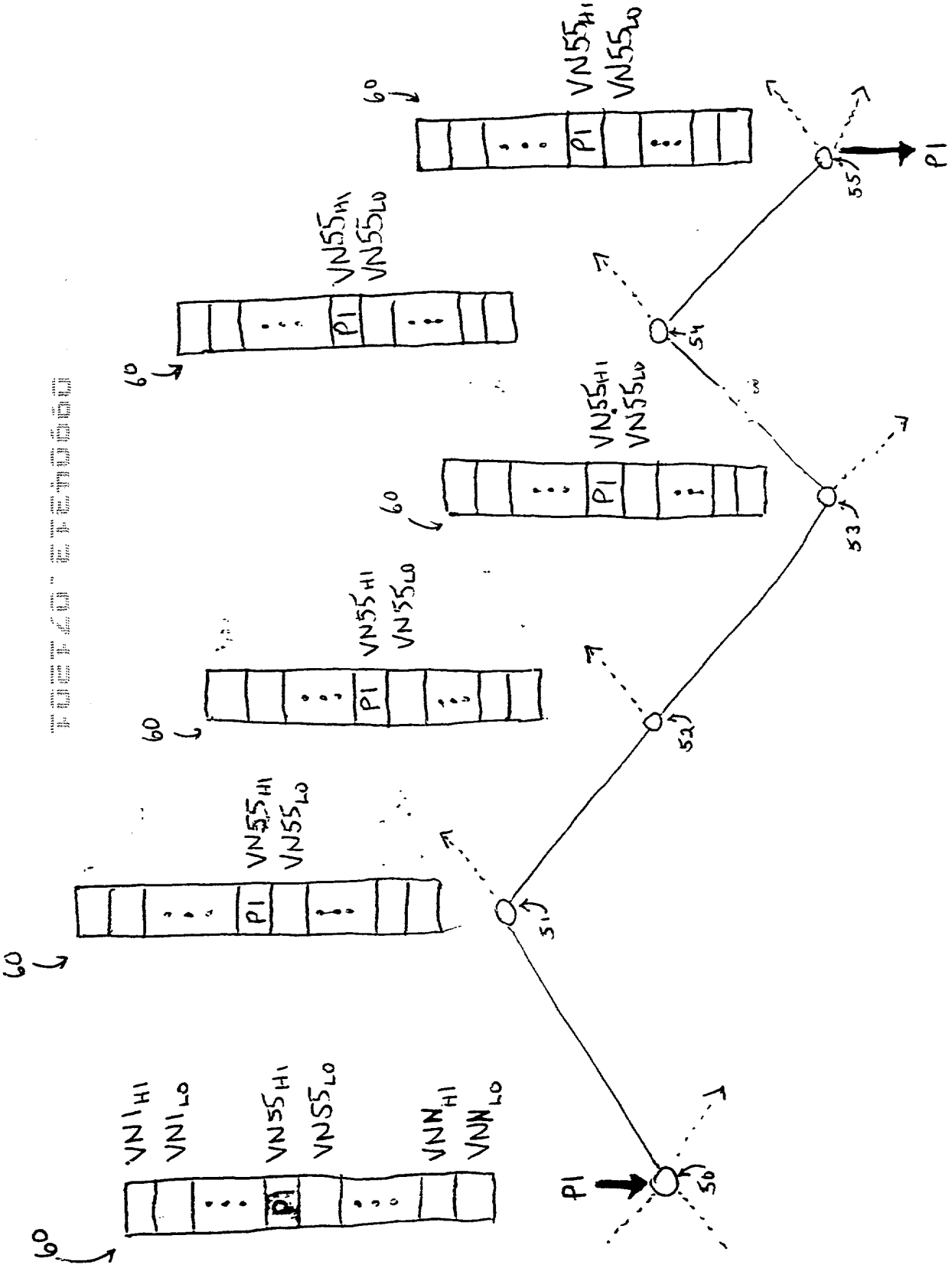


FIG. 6



PRIOR ART

FIG. 7

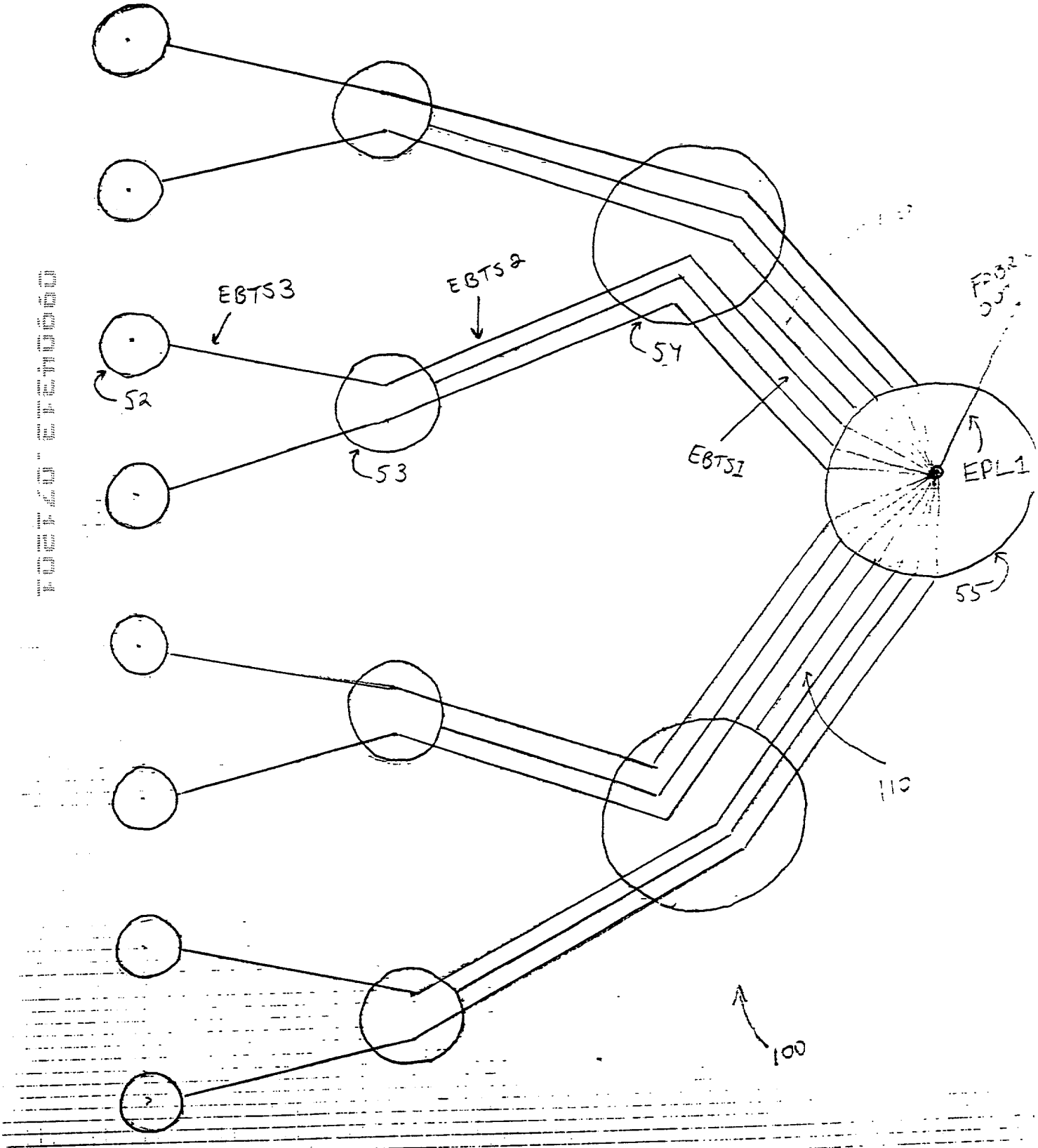


FIG. 8A

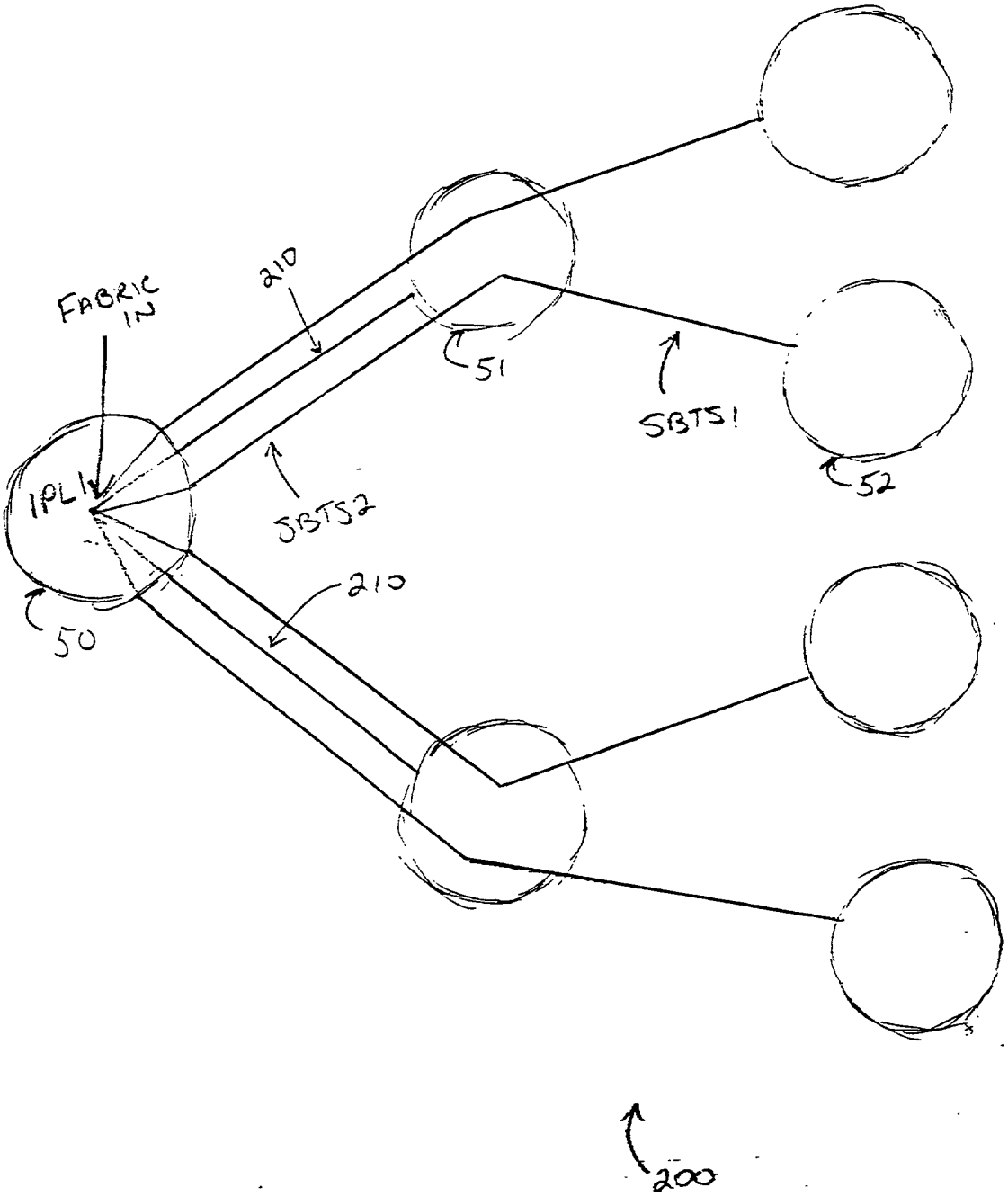


FIG. 8B

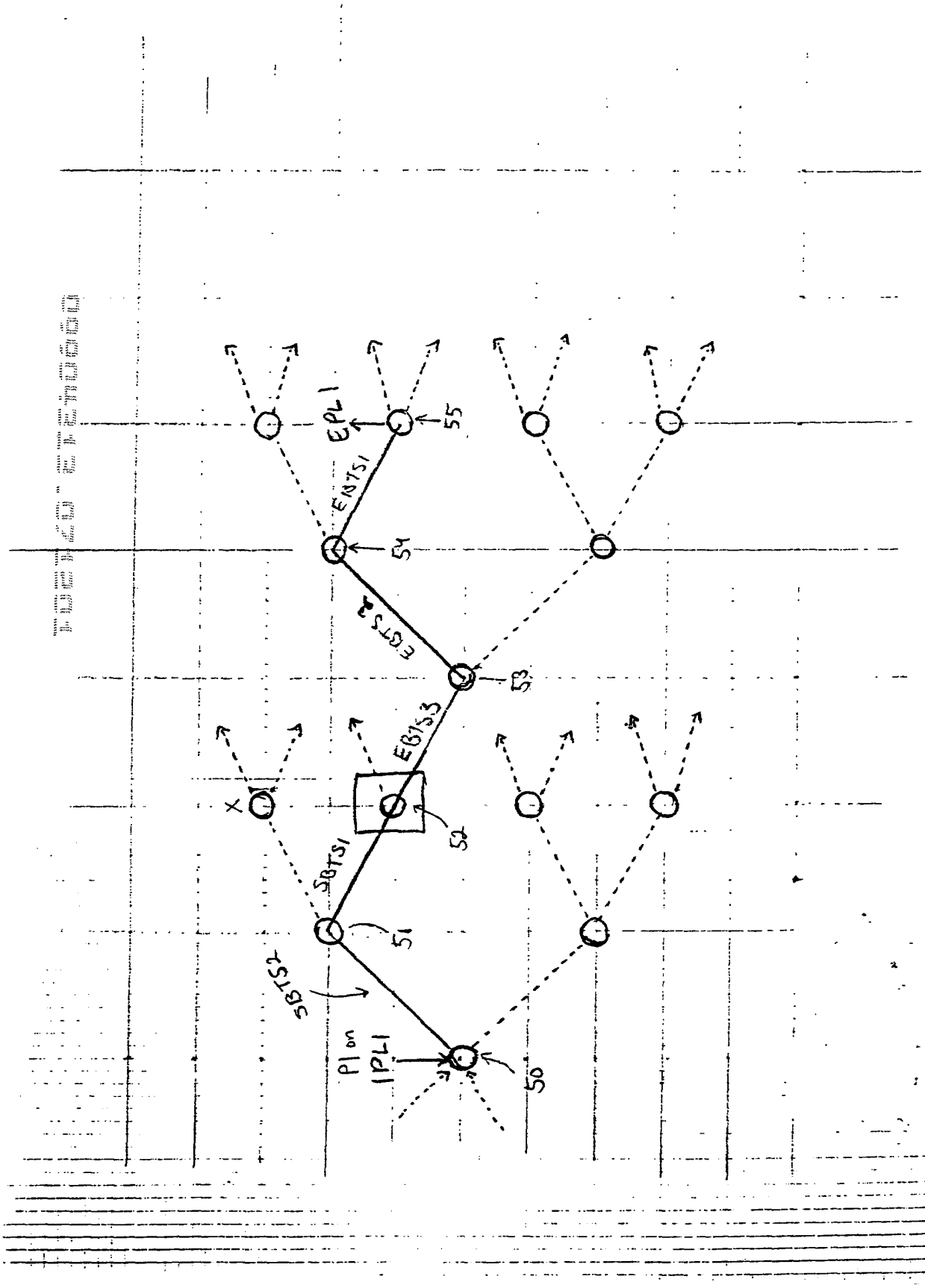


FIG. 9

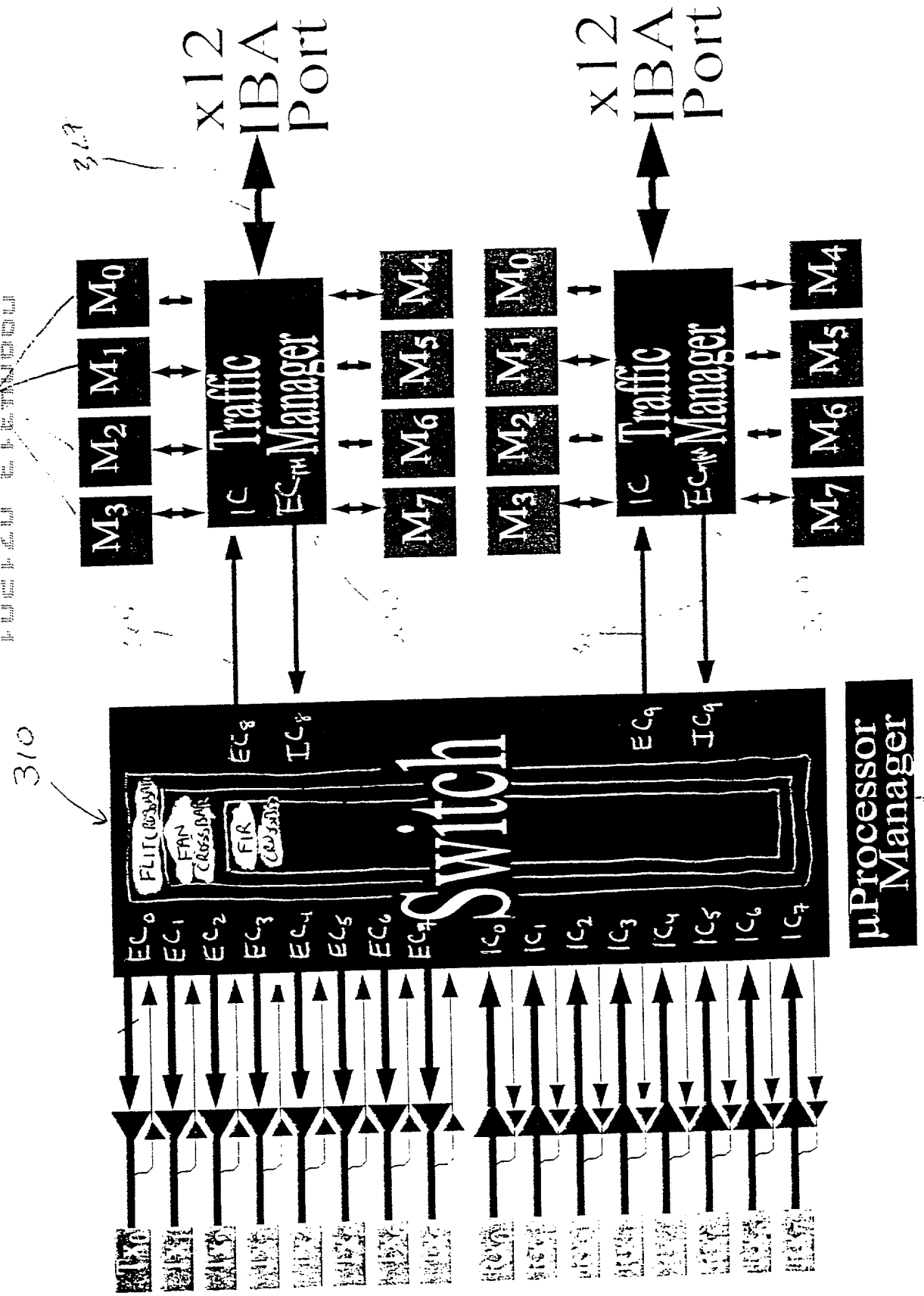

x12 IBA Port
x12 IBA Port
Traffic Manager
Traffic Manager
Switch
µProcessor Manager
310
320
330
340

Fig. 10

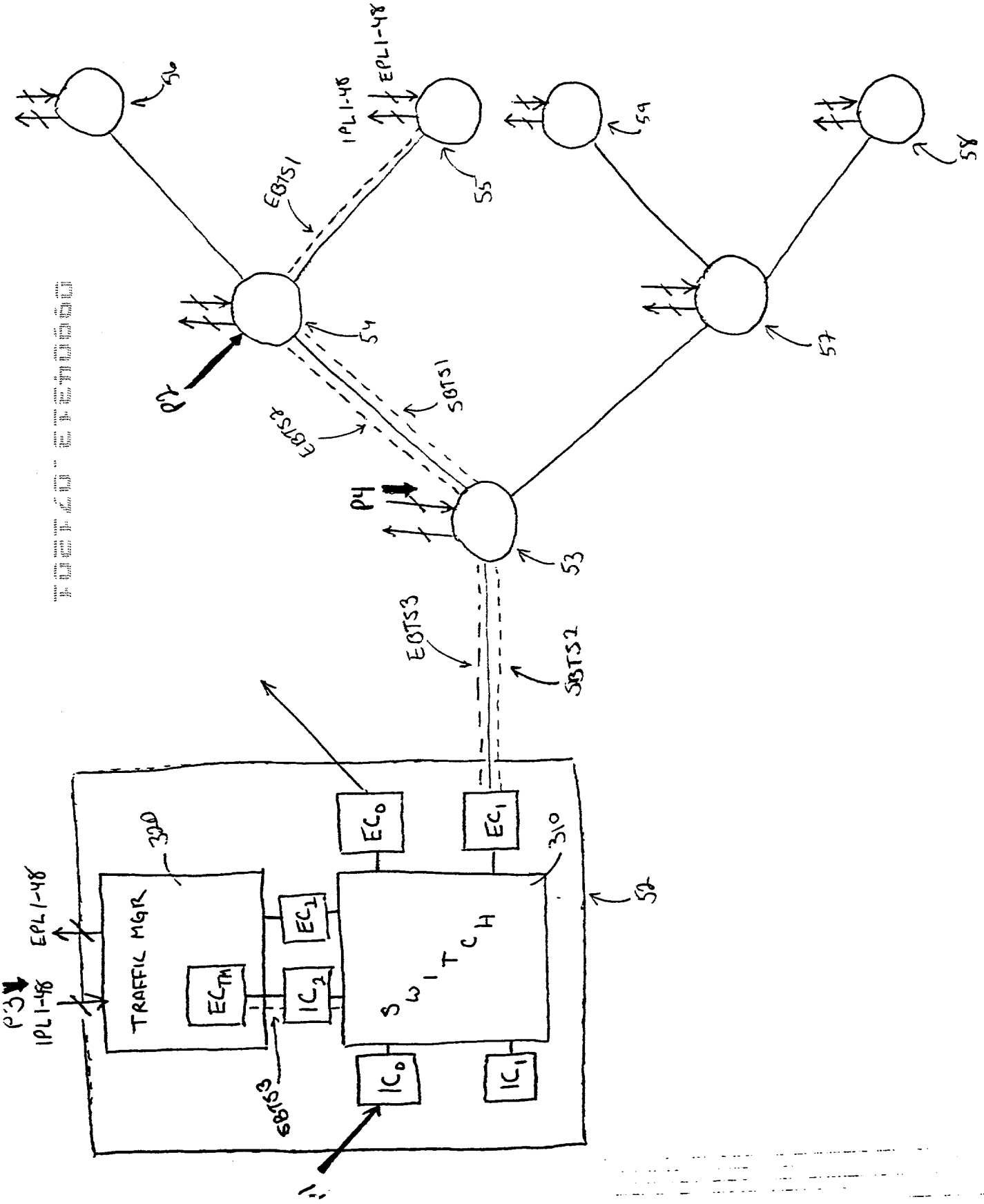

52
IPL1-48
EPL1-48
EOTS1
55
54
P1
EOTS2
SOTS1
P4
53
EOTS3
SOTS2
57
59
58
P3
IPL1-48
EPL1-48
TRAFFIC MGR
320
EC_TM
EC_2
IC_2
EOTS3
EC_0
EC_1
310
SWITCH
IC_0
IC_1
52

FIG. 11A

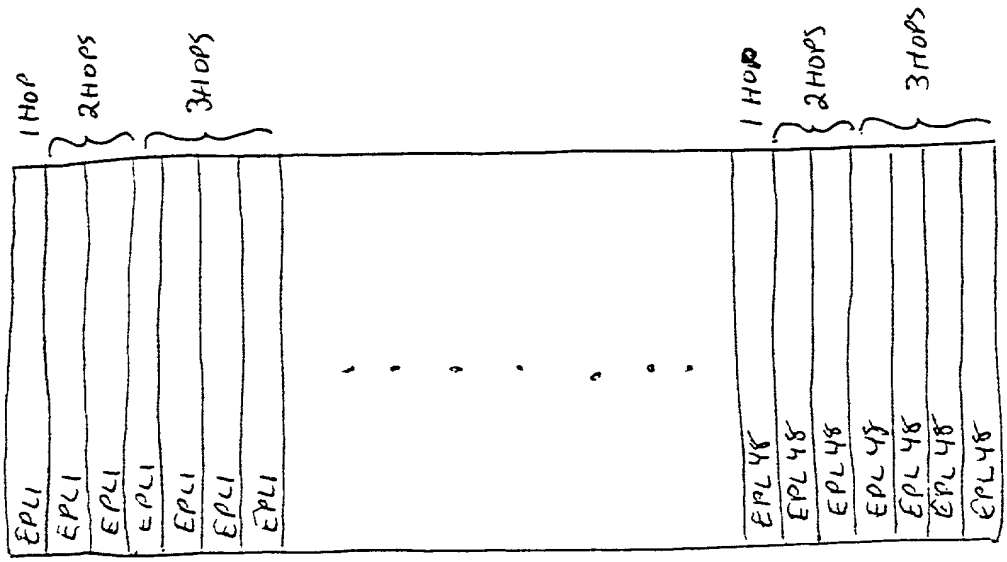


FIG. 11C

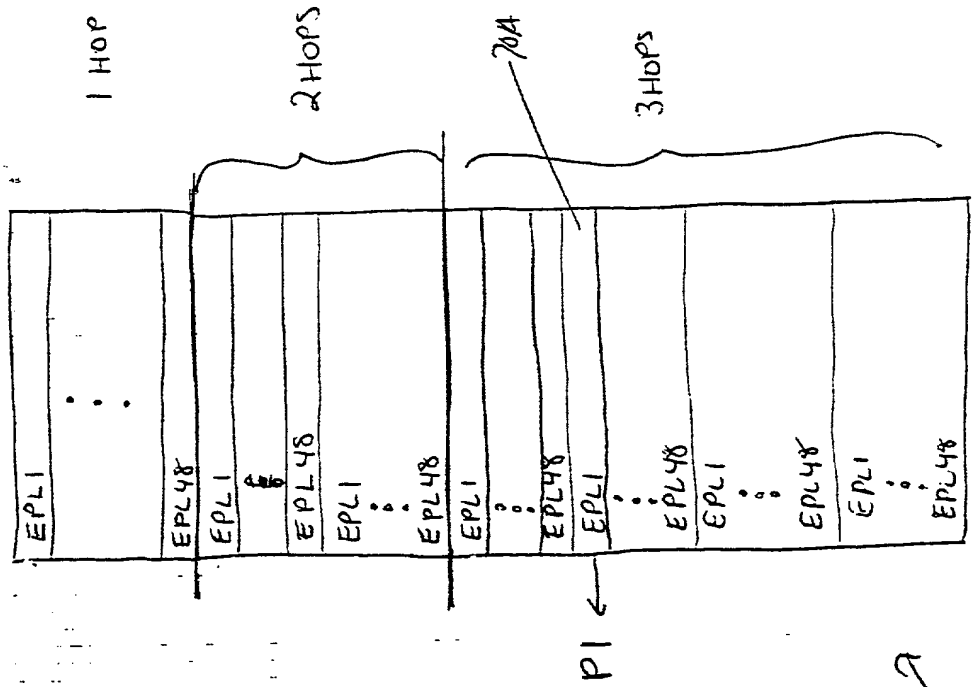


FIG. 11B

PACKET QUEUES FOR EQT SEGMENTS
Applied

PACKET QUEUES FOR SUBSEGMENTS

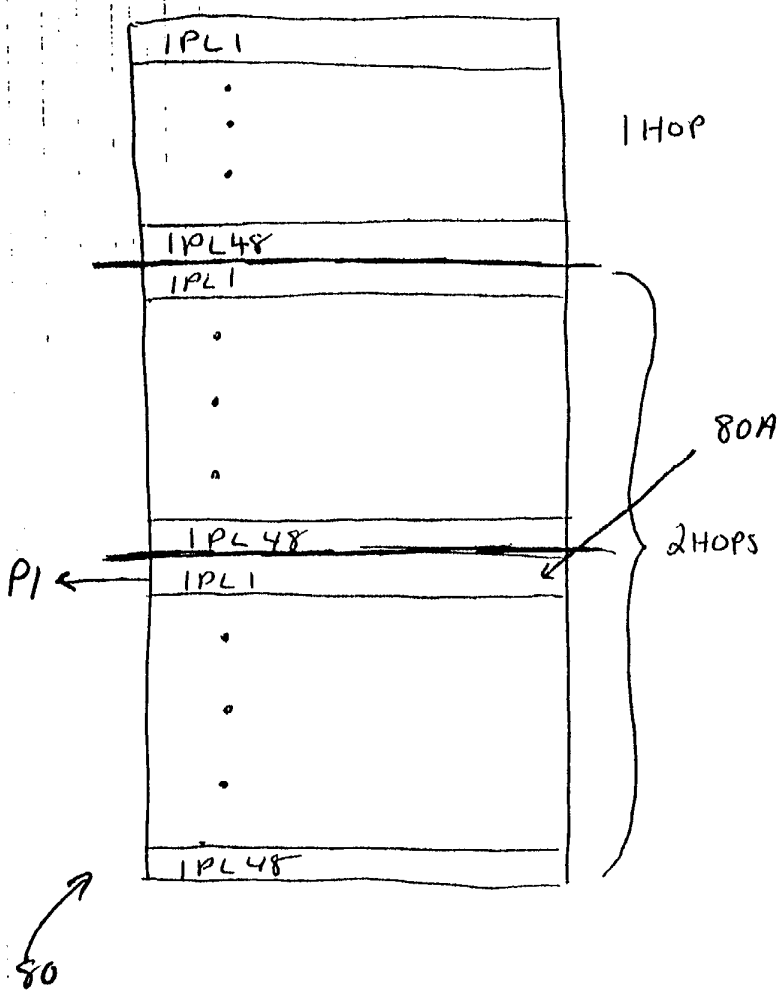


FIG. 11D

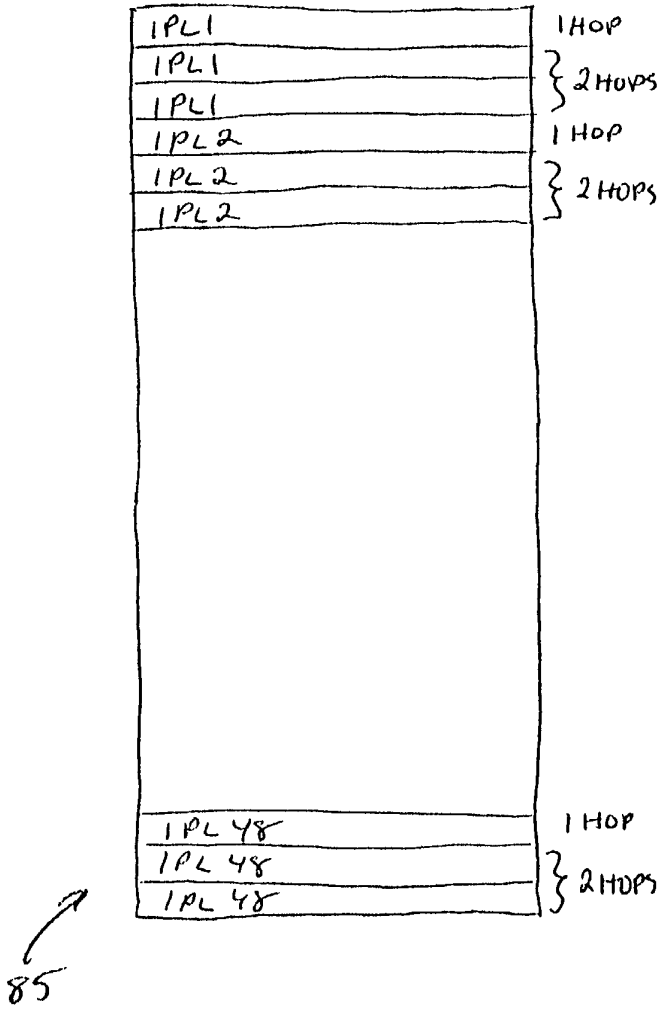


FIG. 11E

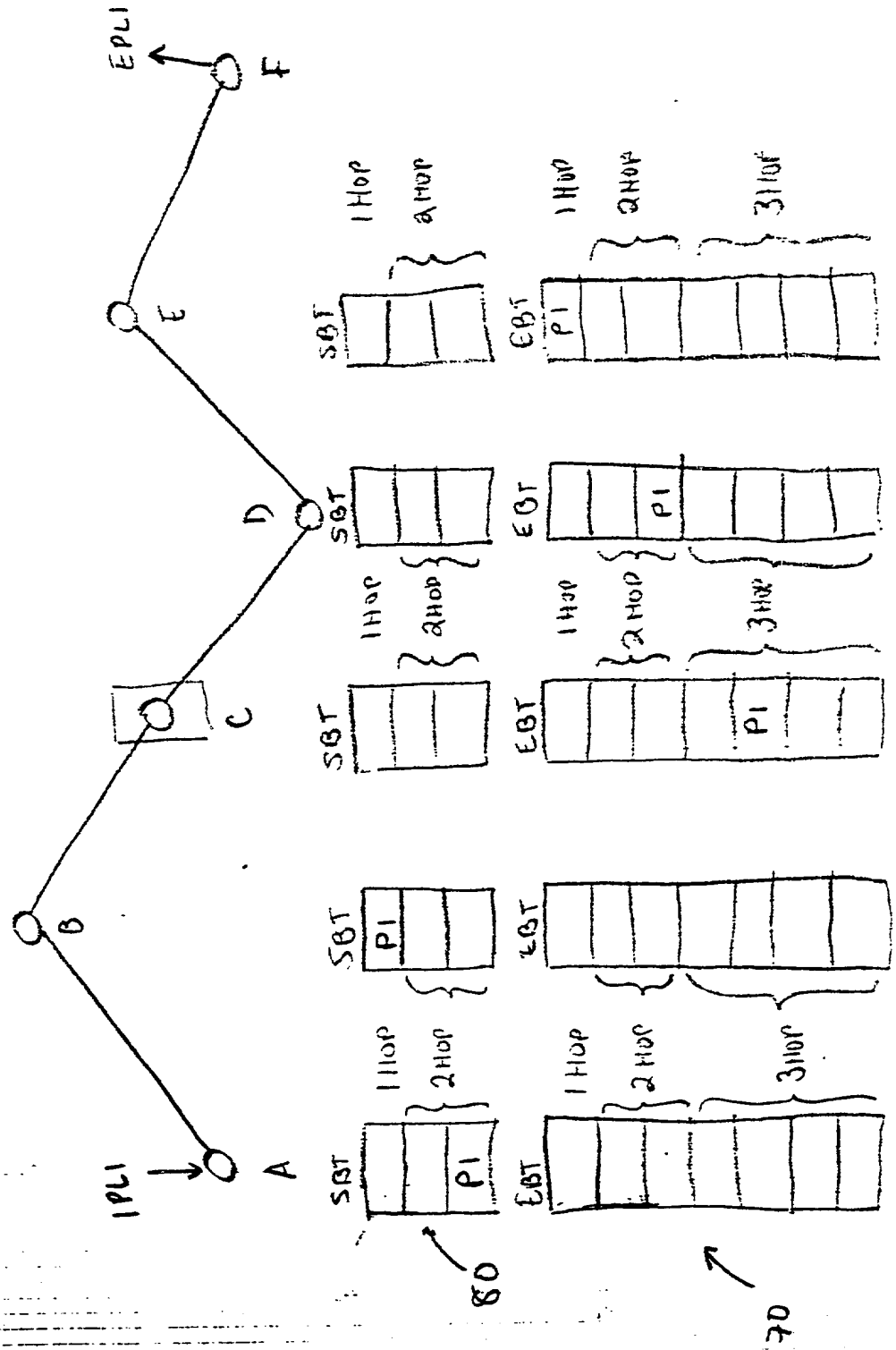


Fig 11

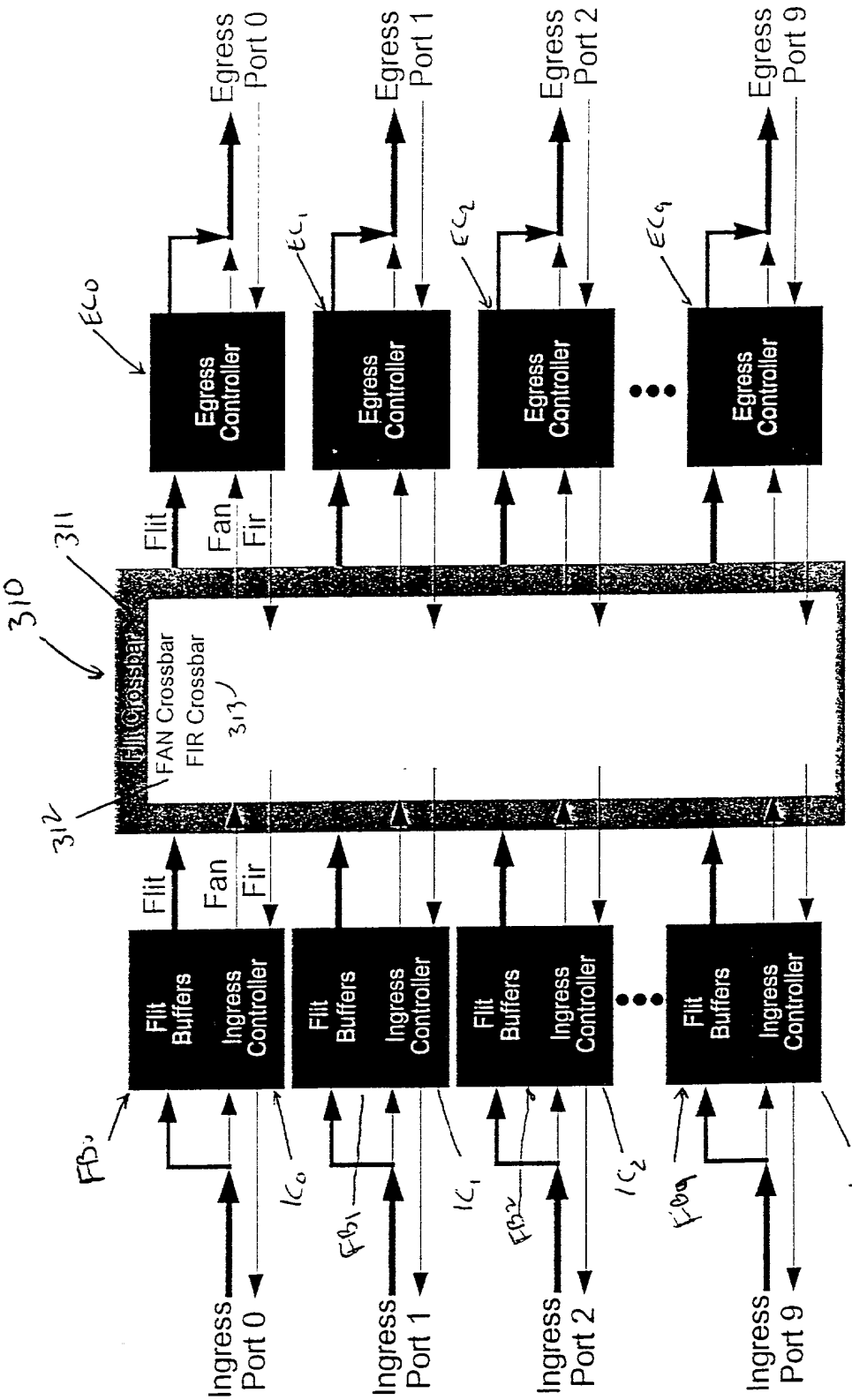

Egress Port 0
Egress Port 1
Egress Port 2
Egress Port 9
Egress Controller
EC0
EC1
EC2
EC9
310
311
Flit Crossbar
FAN Crossbar
FIR Crossbar
313
312
Flit
Fan
Fir
Flit Buffers
Ingress Controller
FB0
FB1
FB2
FB9
IC0
IC1
IC2
IC9
Ingress Port 0
Ingress Port 1
Ingress Port 2
Ingress Port 9

Fig. 12

CONTROL STRUCTURE	SIZE (IN BITS)	DESCRIPTION
IngressPacketState	1280x35=44,800	Each IngressPacketState structure manages the storage of a partially received packet on one of the ingress ports.
EgressLaneState	(128x30=3,480)	Each EgresslaneState structure supplies information used to process received Credits.
AvailableEgressLane	(128x1)	Each flag indicates that a particular lane is available or in use.
FanState	(512x44=22,528)	Each FanState structure holds one FAN waiting to be converted into a FIR and pointers which allow creating a linked list of packets waiting on a particular channel and a linked list of FANs comprising a particular packet.
AvailableFanState	(512x1)	Each flag indicates that a particular local FanState structure is availably or in use.
WaitingForlanes	(2928x1)	Each flag indicates that a particular tunnel segment has a packet ready to be assigned to a lane as soon as one becomes available.
WaitingForFSM	(2928x1)	Each flag indicates that a particular channel has a FAN ready to be converted into a FIR as soon as the EgressController has bandwidth available to perform the conversion.
WaitingForFirFifo	(2304x1)	Each flag indicates that a particular lane has a FAN ready to convert into a FIR as soon as room in the FIR FIFO becomes non-full.
SegmentPointer	(2938x13=38,194)	Each SegmentPointer points to a a queue of packets waiting on a tunnel segment.

FIG. 13

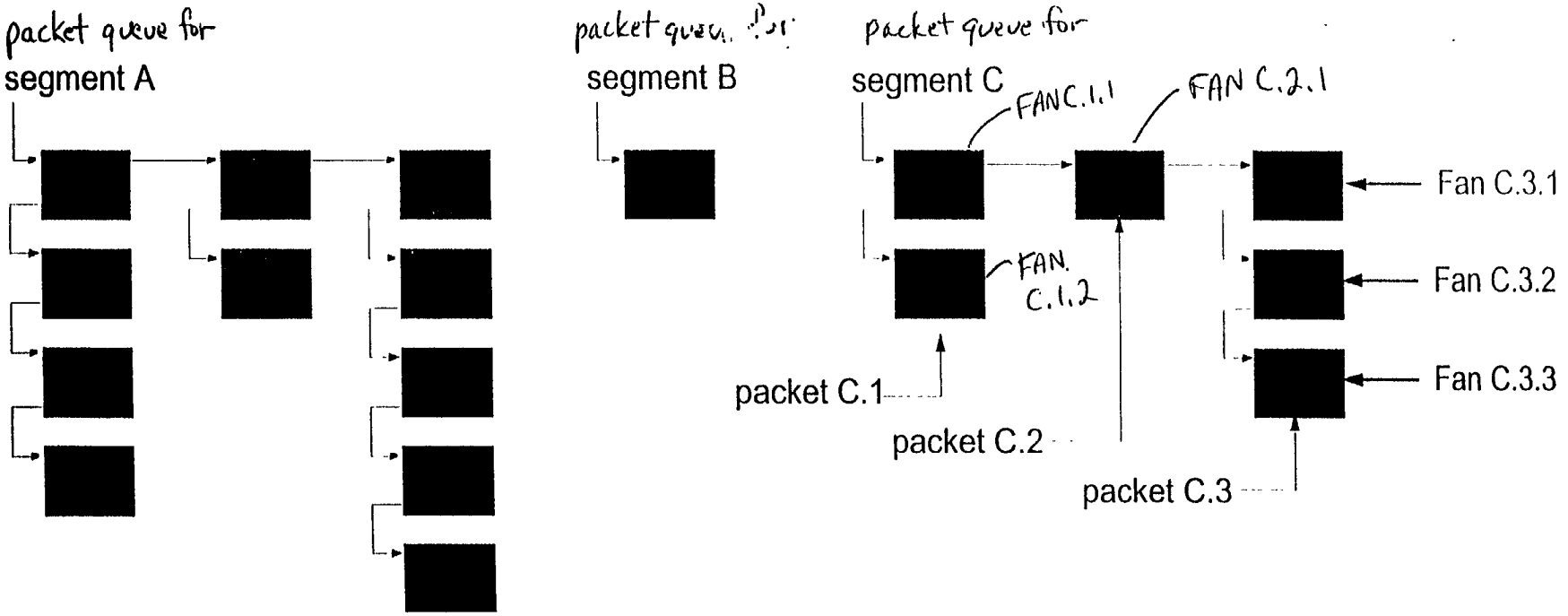

packet queue for
segment A
packet queue for
segment B
packet queue for
segment C
FANC.1.1
FAN C.2.1
Fan C.3.1
FAN.
C.1.2
Fan C.3.2
Fan C.3.3
packet C.1
packet C.2
packet C.3

FIG. 14

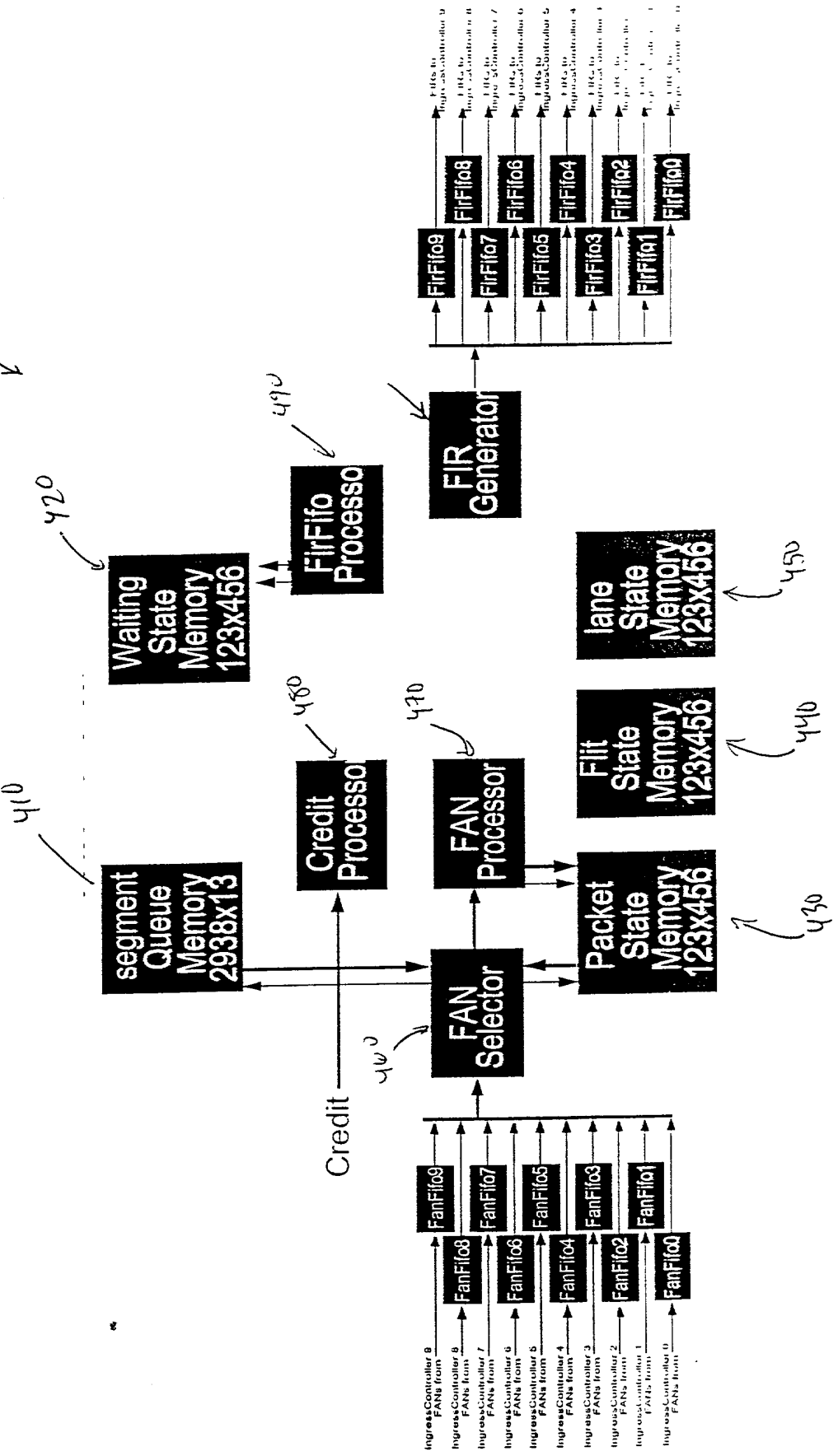

400
410
segment Queue Memory 2938x13
420
Waiting State Memory 123x456
430
Packet State Memory 123x456
440
Flit State Memory 123x456
450
Iane State Memory 123x456
460
Credit Processo
470
FAN Processor
480
FirFifo Processo
490
FIR Generator
FAN Selector
Credit
FanFifo9
FanFifo8
FanFifo7
FanFifo6
FanFifo5
FanFifo4
FanFifo3
FanFifo2
FanFifo1
FanFifo0
FirFifo9
FirFifo8
FirFifo7
FirFifo6
FirFifo5
FirFifo4
FirFifo3
FirFifo2
FirFifo1
FirFifo0

Fig. 15